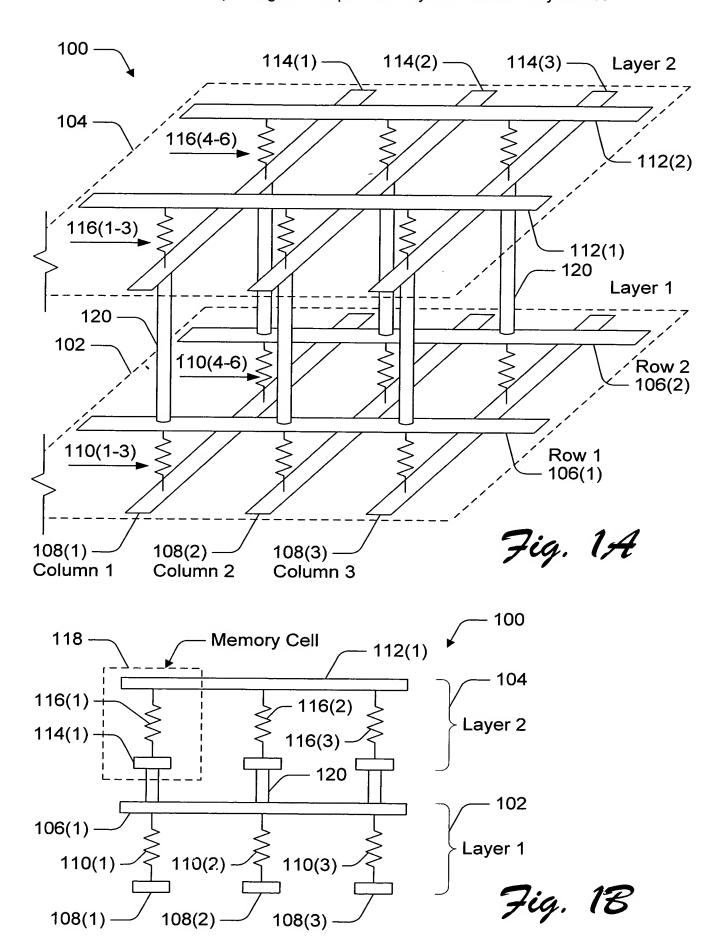
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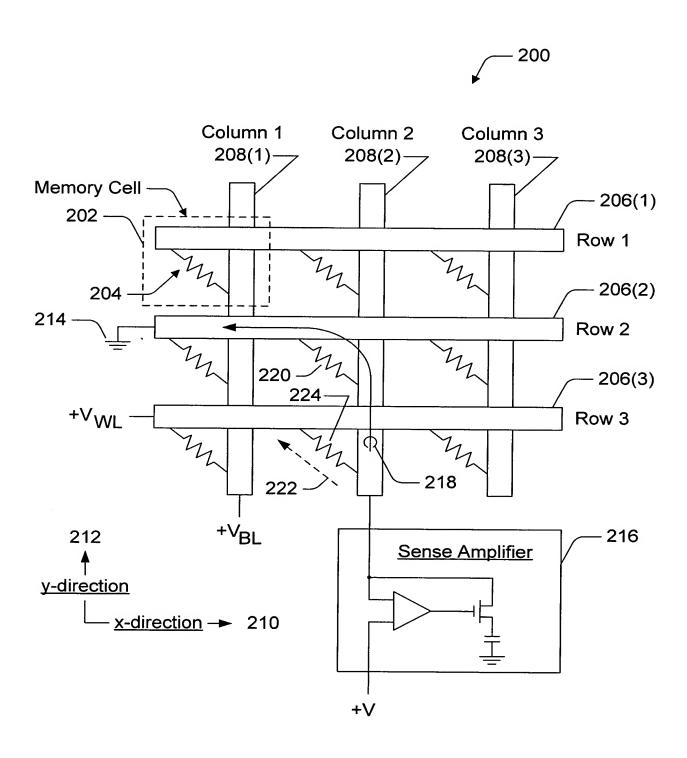


Fig. 2

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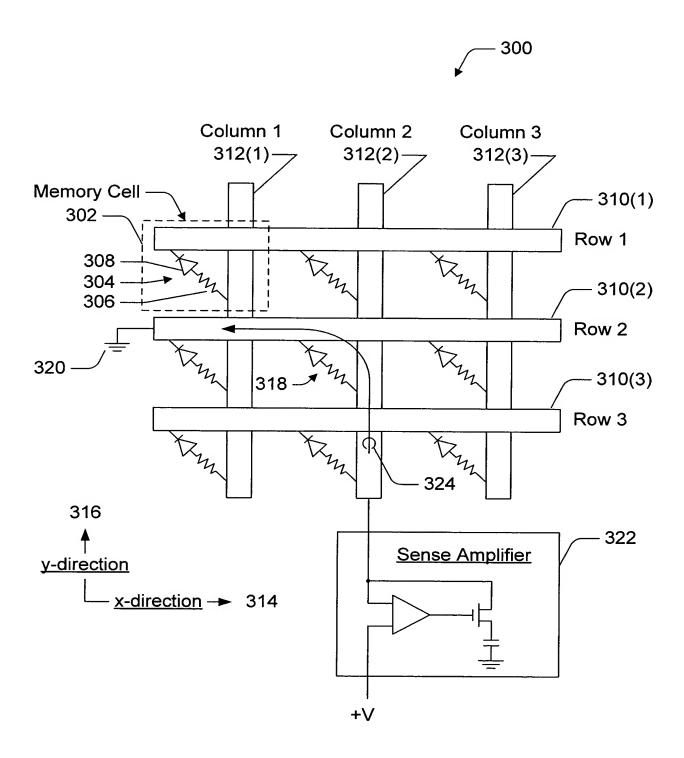
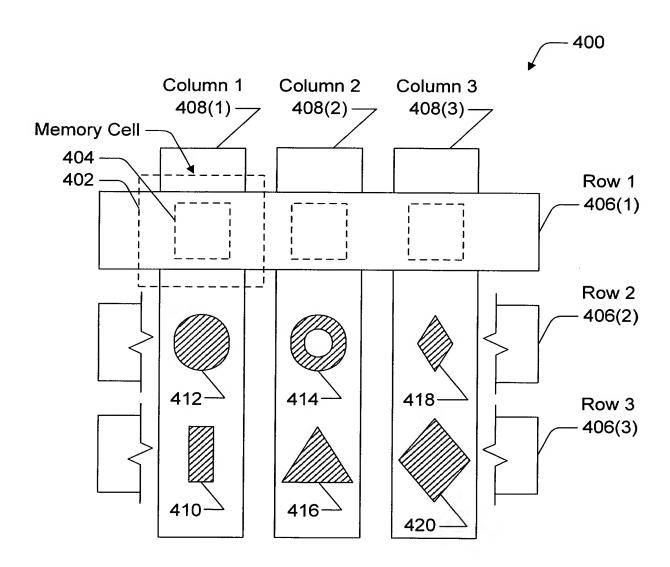


Fig. 3

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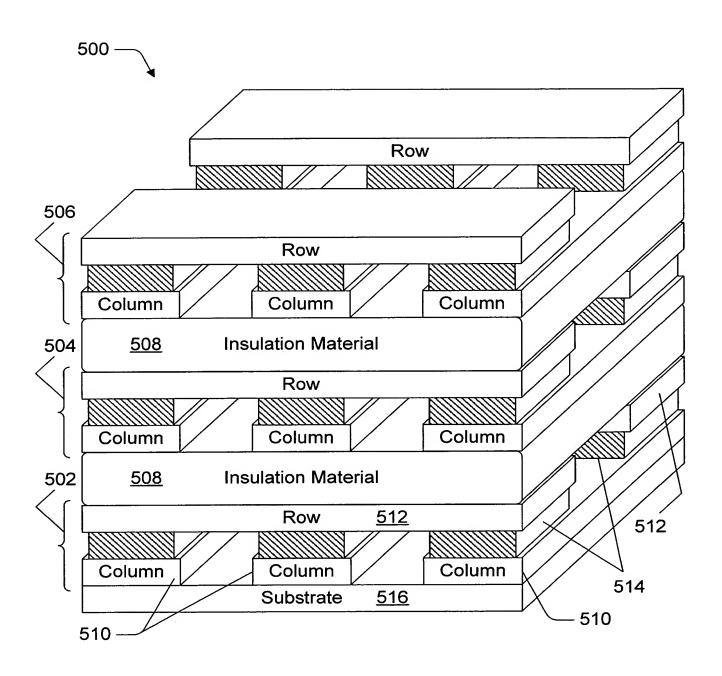
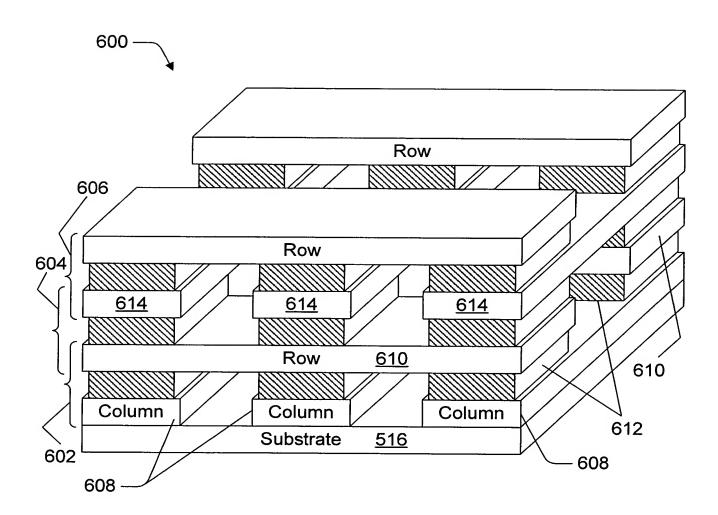


Fig. 5

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Title: Multiple Logical Bits per Memory Cell in a Memory Device

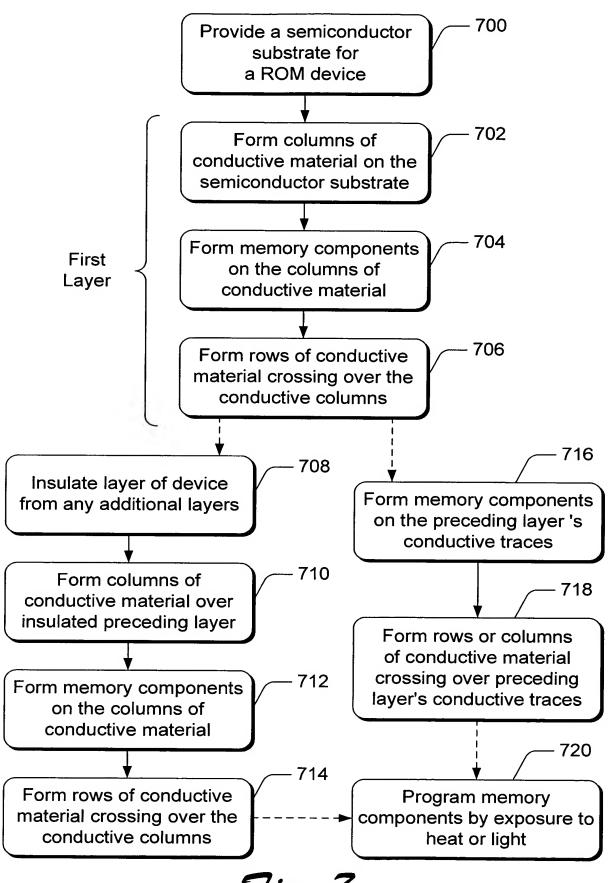


Fig. 7